鴻鎵科技
GaN Power Tech

650 V GaN FET in DFN 8x8

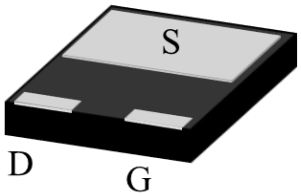
Description

The GPT65Z3YMR 650 V, 245 mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies-offering superior reliability and performance.

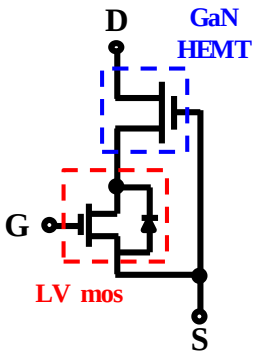
The GaN offers improved efficiency over silicon, through lower gate charge, lower crossover loss, and smaller reverse recovery charge.

Ordering Information

Part Number	Package	Package Configuration
GPT65Z3YMR	DFN8080	Source



GPT65Z3YMR DFN 8x8



Cascode Device Structure

Features

- JEDEC qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - — Intrinsic lifetime tests
  - — Wide gate safety margin
  - — Transient over-voltage capability
- Enhanced inrush current capability Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- AC-DC bridgeless totem-pole PFC designs
  - — Increased power density
  - — Reduced system size and weight
  - — Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

GPT65Z3YMR	
V_{DSS}	650 V
$R_{DS(on)}$	245 mΩ
$Q_{RR,}$ typ	40 nC
$Q_{G,}$ typ	22 nC

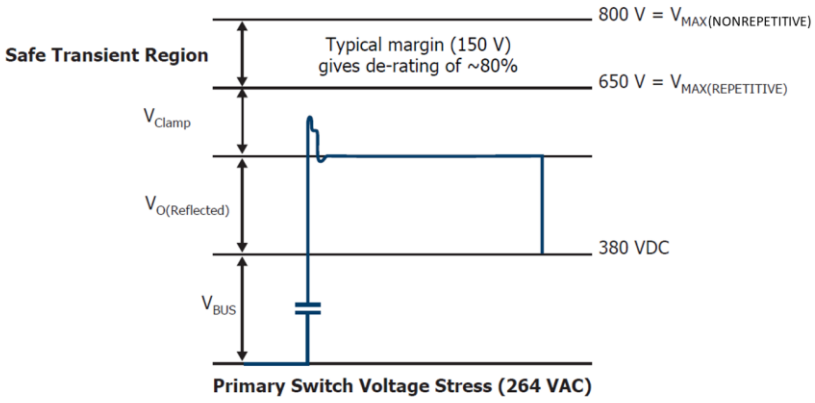
ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Limited Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
$V_{(TR)DSS}$	Transient Drain to Source Voltage[a]		800	V
V_{GSS}	Gate to Source Voltage		±20	V
P_D	Maximum Power Dissipation @T_C = 25°C		38	W
I_D	Continuous Drain Current	T_C = 25°C	9	A
		T_C = 100°C	6	A
I_{DM}	Pulsed Drain Current	Pulse Width = 10 μs	31	A
T_C	Operating Temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage Temperature		-55 to +150	°C
T_{SOLD}	Soldering Peak Temperature[b]		260	°C

Notes:

a. In off-state, spike duty cycle D<0.01, spike duration <20μs

b. Relow MSL3



THERMAL CHARACTERISTICS

Symbol	Parameter	Typical	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient[c]	50	°C/W

Notes:

c. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6 cm^2 copper area and 70 μm thickness)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Forward Device Characteristics						
$V_{(BL)DSS}$	Maximum Drain to Source Voltage	V_{GS} = 0 V	650			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 500 μA	1	1.6	2.5	V
$R_{DS(on)eff}$	Drain to Source On Resistance	V_{GS} = 8 V, I_D = 4 A		245	300	mΩ
		V_{GS} = 8 V, I_D = 4 A, T_J = 150°C		500		
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0 V, V_{DS} = 650 V		10	20	μA
		V_{GS} = 0 V, V_{DS} = 650 V, T_J = 150°C		50		
I_{GSS}	Gate to Source Forward Leakage Current	V_{GS} = 20 V			150	nA
	Gate to Source Reverse Leakage Current	V_{GS} = -20 V			-150	
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 650 V, f=1 MHz		500		pF
C_{OSS}	Output Capacitance			20		pF
C_{RSS}	Reverse Transfer Capacitance			2		pF
$C_{o(er)}$	Output Capacitance, Energy Related	V_{GS} = 0 V, V_{DS} = 0 V~650 V		25		pF
$C_{o(tr)}$	Output Capacitance, Time Related			45		pF
Q_G	Total Gate Charge	V_{GS} = 0 V~12 V, V_{DS} = 400 V, I_D =5.5 A		22		nC
Q_{GS}	Gate to Source Charge			3		
Q_{GD}	Gate to Drain Charge			3.5		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 0 V~650 V		32		nC
$t_{D(on)}$	Turn-on Delay	V_{GS} = 0 V~12 V, V_{DS} = 400 V, I_D = 3 A , R_g = 30 Ω		20		ns
t_R	Rise Time			7		
$t_{D(off)}$	Turn-off Delay			80		
t_F	Fall Time			6		
Reverse Device Characteristics						
V_{SD}	Reverse Voltage	V_{GS} = 0 V, I_S = 5 A		1.5		V
		V_{GS} = 0 V, I_S = 2 A		1.0		
t_{RR}	Reverse Recovery Time	I_S = 3 A, V_{DS} = 400 V, di/dt = 1000 A/μs		12		ns
Q_{RR}	Reverse Recovery Charge			40		nC

LAYOUT GUIDELINES

The layout of GaN FETs is very important for performance and EMI due to the GaN FETs are normally operated under high voltage and high current. Figure 22 and Figure 23 show an example of a good power layout loop:

POWER-LOOP INDUCTANCE

The GaN FET has operated at a high transient current (di/dt) state. Therefore, the ringing, EMI, and voltage stress on GaN FET could be reduced by minimizing the inductance of the loop.

1. GND with a large area copper plane provides a low inductance ground for the GaN FET (Q1).
2. The power device GaN FET (Q1), diode (D3), and transformer (T1) are placed as close as possible to reduce the inductance.
3. The power device GaN FET (Q1) and resistor (R3) are placed as close as possible to reduce inductance and avoid abnormal switching.
4. Resistor (R3) and decoupling capacitor (C1) are placed as close as possible to minimize the current path and reduce the inductance.

SWITCHING NODE CAPACITANCE

GaN devices have very low switching losses due to its low output capacitance and fast switching with high transient voltage (dv/dt). Therefore, additional capacitance on the output node should be minimized.

1. Shrinking the area of copper reduces the extra capacitance of the switching node.
2. Switching Node Trace should not overlap with Power plane and GND plane.
3. The copper plane of the Switching Node is not used for heat dissipation of the circuit board.

TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

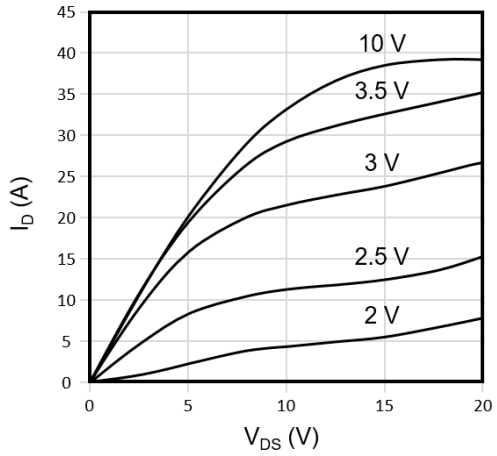


Figure 1. Typical Output Characteristics T_J = 25°C

Parameter: V_{GS}

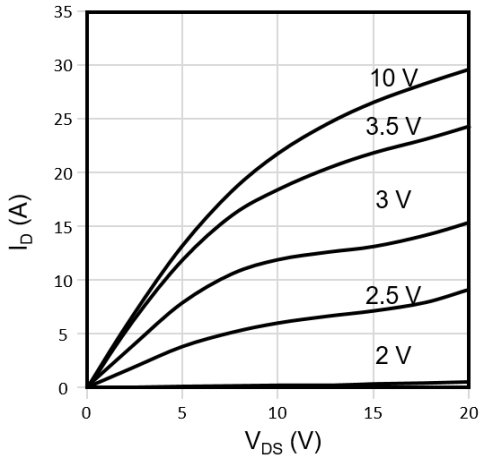


Figure 2. Typical Output Characteristics T_J = 150°C

Parameter: V_{GS}

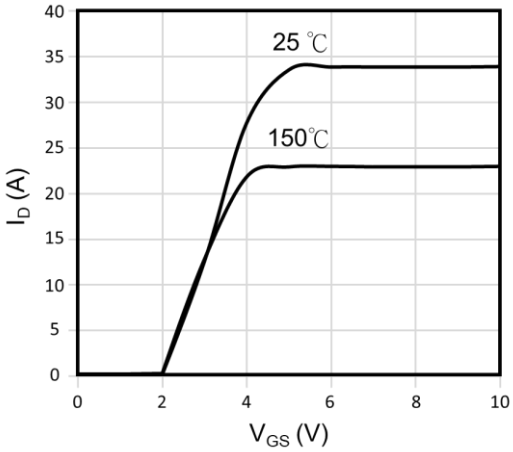


Figure 3. Typical Transfer Characteristics

V_{DS} = 10 V, parameter: T_J

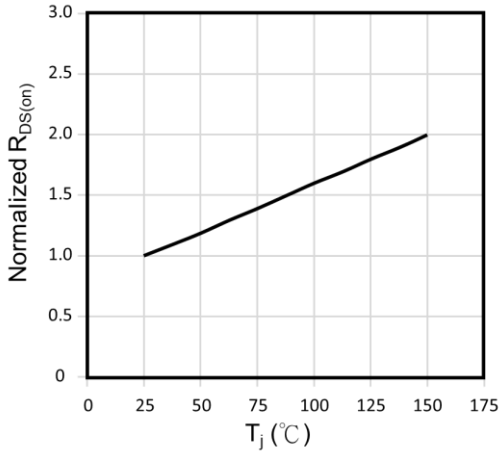


Figure 4. Normalized On-resistance

I_D = 4 A, V_{GS} = 8 V

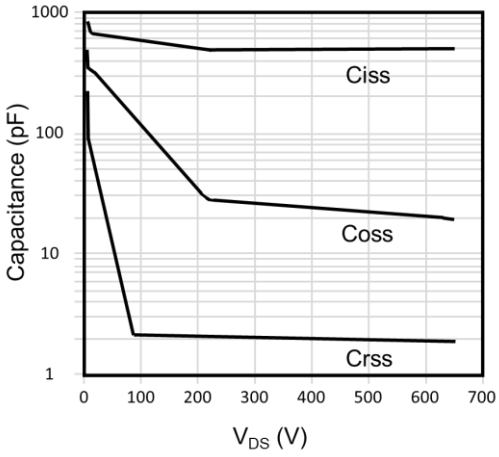


Figure 5. Typical Capacitance

V_{GS} = 0 V, f = 1 MHz

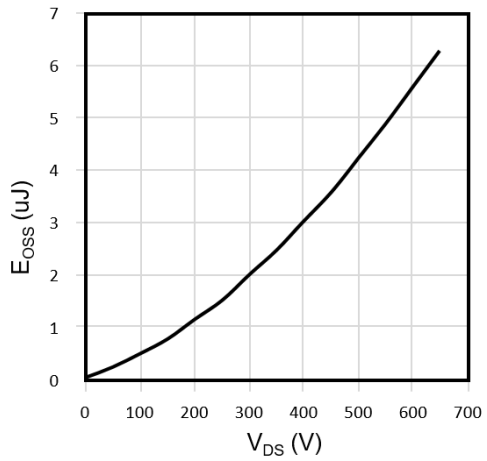


Figure 6. Typical C_{OSS} Stored Energy

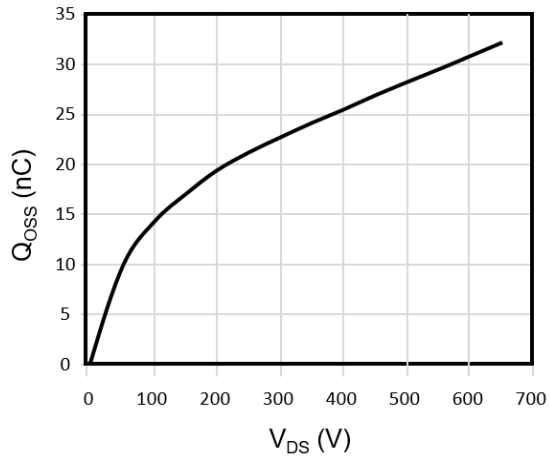


Figure 7. Typical Q_{OSS}

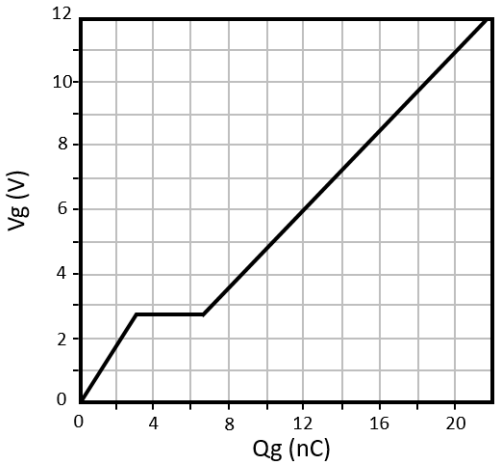


Figure 8. Typical Gate Charge

I_{DS} = 5.5 A, V_{DS} = 400 V

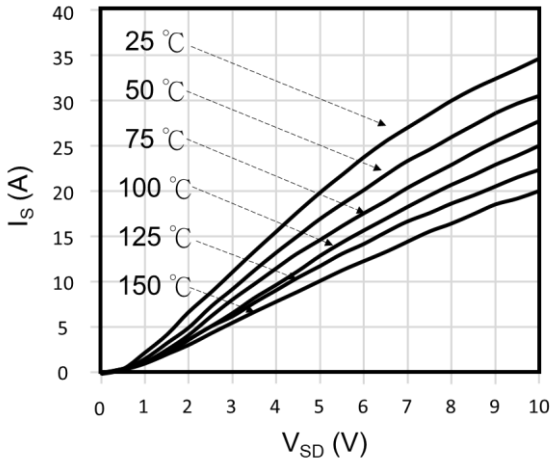


Figure 9. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter T_J

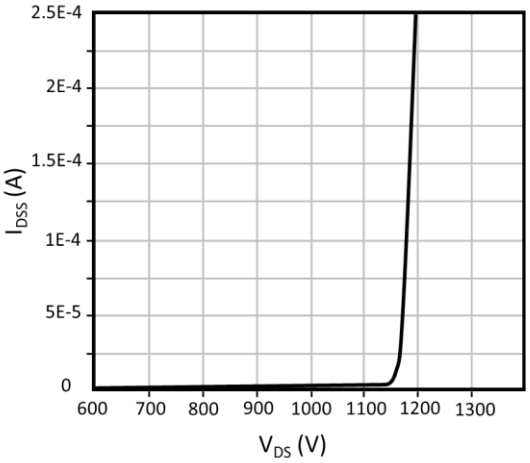


Figure 10. Drain-Source Breakdown Voltage

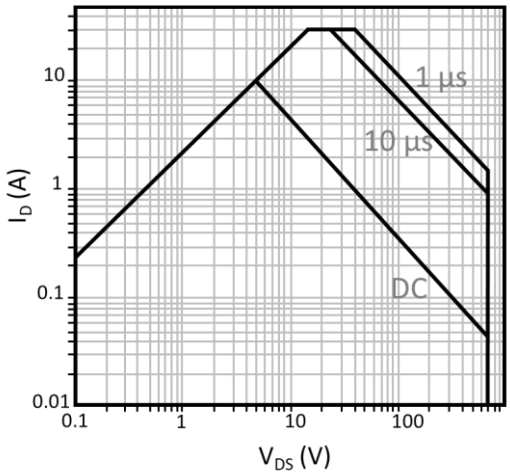


Figure 11. Safe Operating Area T_C = 25°C

(calculated based on thermal limit)

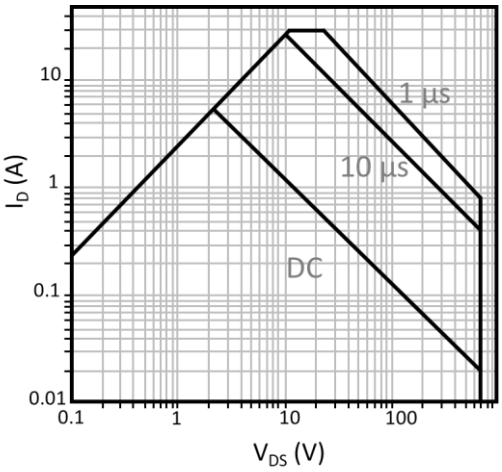


Figure 12. Safe Operating Area T_C = 80°C

(calculated based on thermal limit)

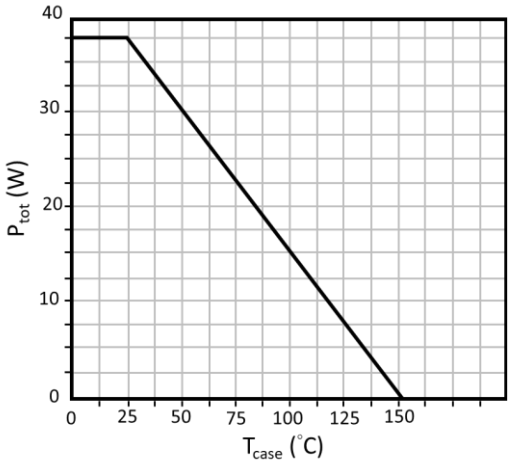


Figure 13. Power Dissipation

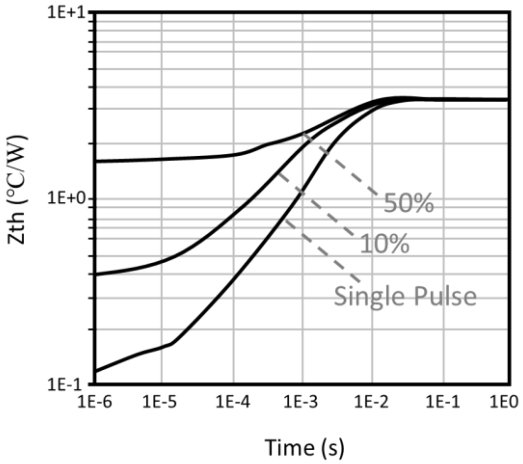


Figure 14. Transient Thermal Resistance

TEST CIRCUITS AND WAVEFORMS

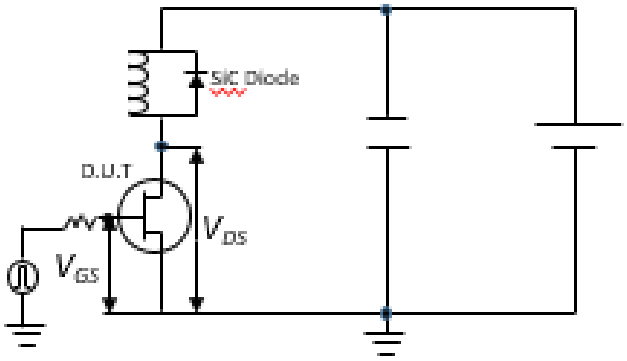


Figure 15. Switching Time Test Circuit

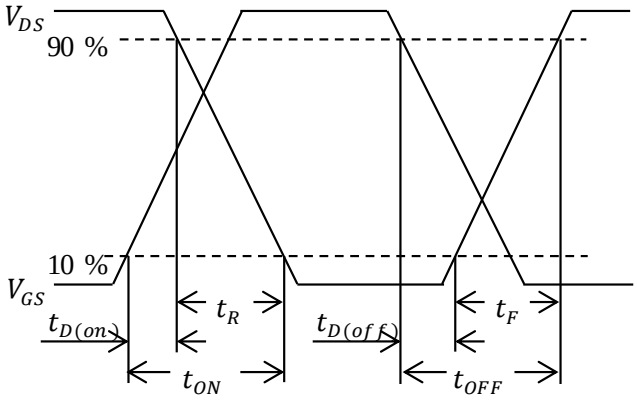


Figure 16. Switching Time Waveform

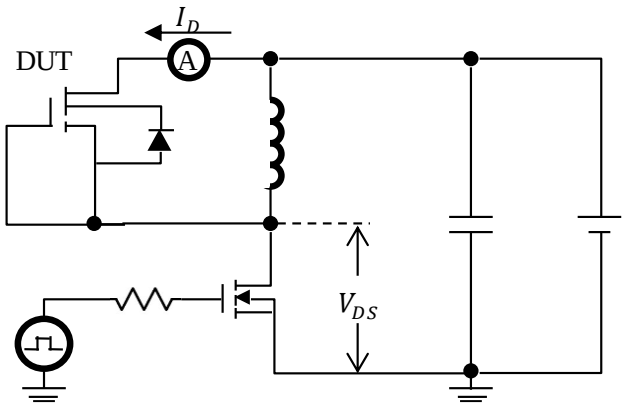


Figure 17. Diode Characteristics Test Circuit

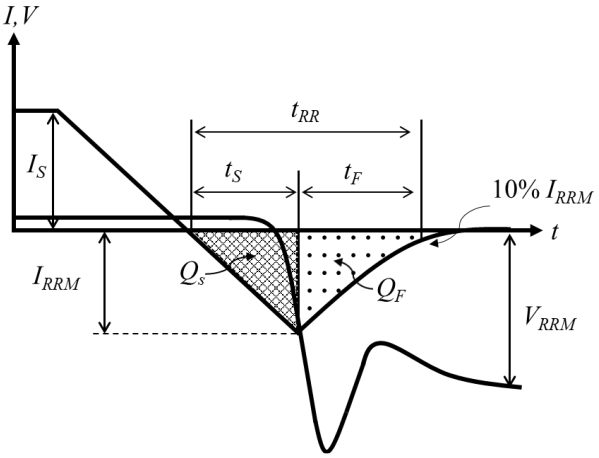


Figure 18. Diode Recovery Waveform

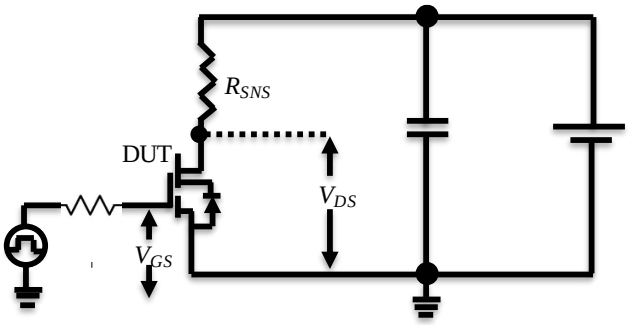


Figure 19. Dynamic $R_{DS(ON)eff}$ Test Circuit

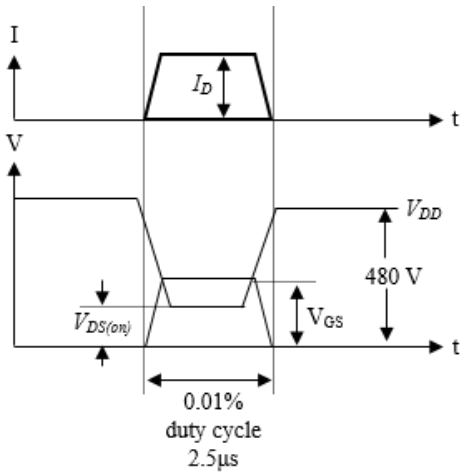


Figure 20. Dynamic $R_{DS(ON)eff}$ Waveform

TYPICAL APPLICATION

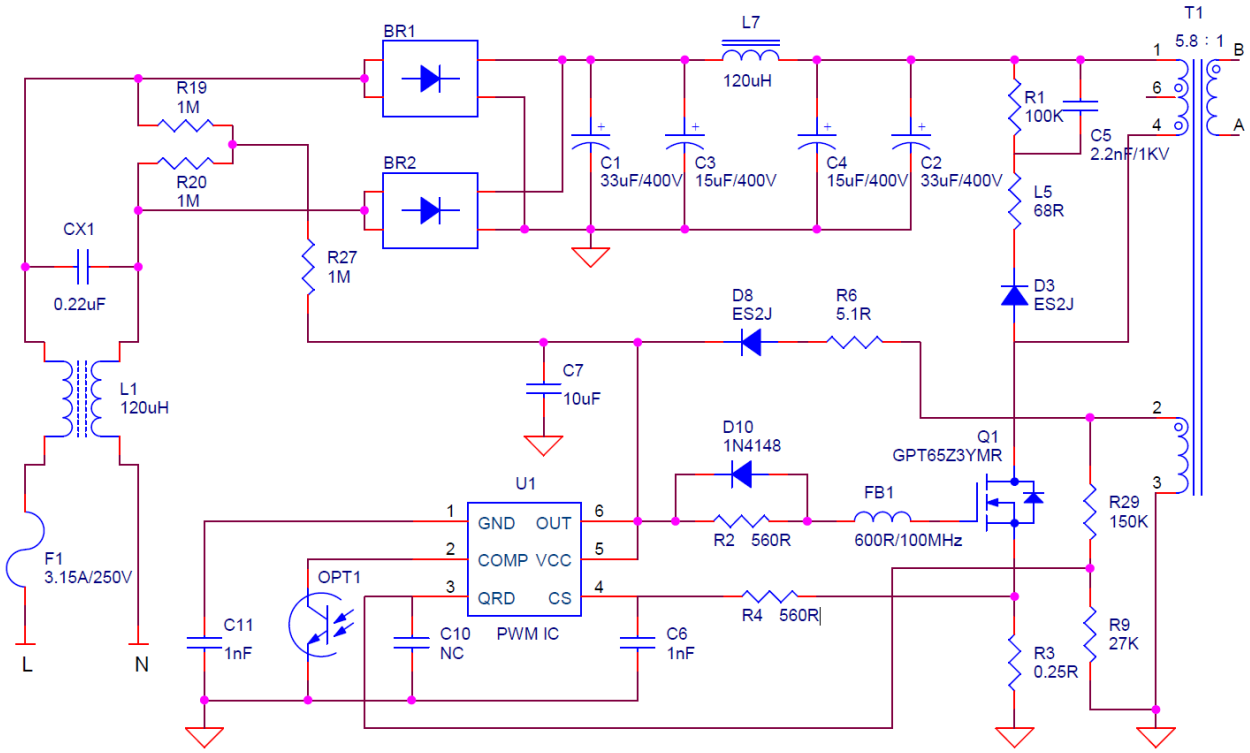


Figure 21. Typical Application Schematic

LAYOUT EXAMPLE

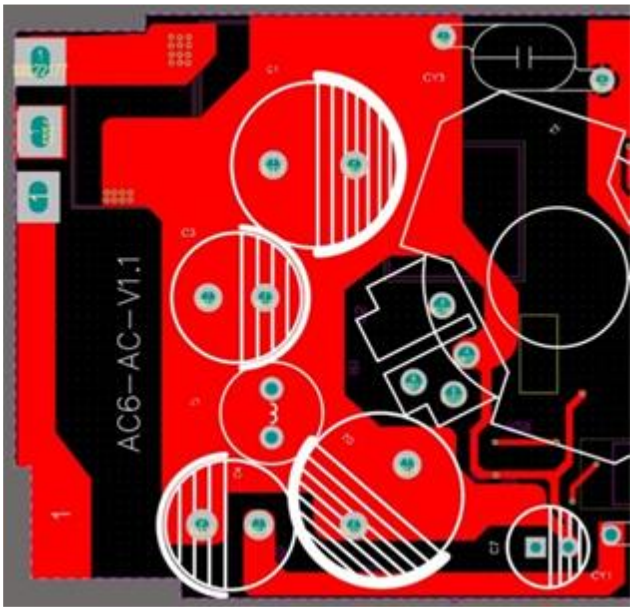


Figure 22. Top Layer for FR4 1.6mm

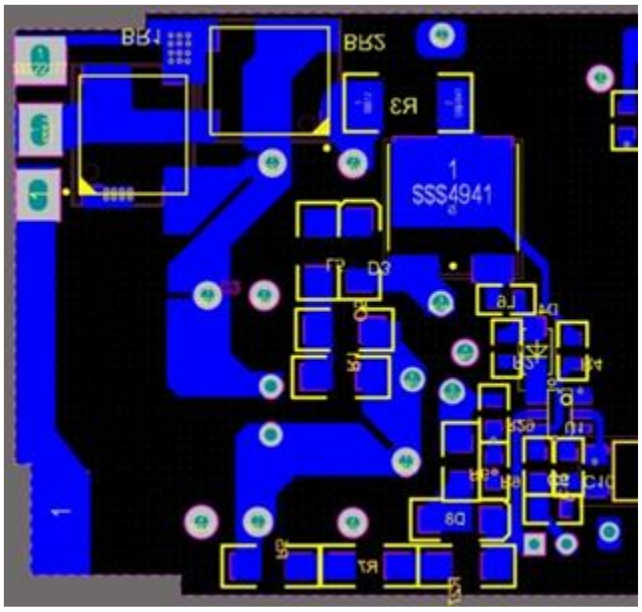
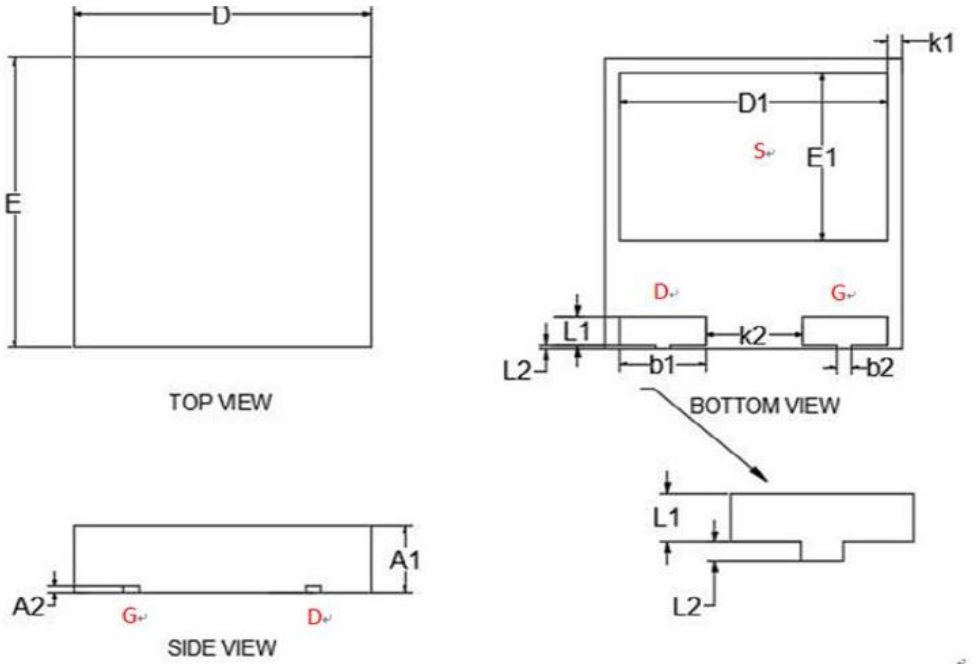


Figure 23. Bottom Layer for FR4 1.6mm

PACKAGE OUTLINE



DFN 8x8 PACKAGE

SYMBOL	Dimensions in mm		
	Min	Nom	Max
A1	0.850	0.900	0.950
A2	0.185	0.203	0.230
D	7.000	8.000	9.000
E	7.950	8.000	8.050
D1	7.050	7.200	7.350
E1	4.450	4.600	4.750
K1	0.375	0.400	0.425
K2	2.575	2.600	2.625
B1	2.250	2.300	2.350
B2	0.375	0.400	0.425
L1	0.700	0.800	0.900
L2	0.075	0.100	0.125

REVISION HISTORY

Version	Date	Changes
1.0	2022.4.7	Preliminary datasheet.
2.0	2022.5.20	Update test circuits.
3.0	2022.9.30	Added application note on page 8 and page 9.
3.1	2022.10.24	Update figure 21 on page 9 and typesetting.